REMARKS

Claims 60-64 have been canceled. Claims 29-32, 34-39, 41, 44-47, 49, 51-59 and 65 are currently pending in this application. Applicant reserves the right to pursue the original and other claims in this and other applications. Applicant respectfully requests reconsideration in light of the above amendments and the following remarks.

The claimed invention relates to an electropolished patterned metal layer formed as a lower electrode of a capacitor, which may be part of a semiconductor device, such as a memory cell, or a processor-based system. The electropolished metal layer of the claimed invention allows for high resolution patterning with increased processing accuracy in the patterning of noble metals. Specification, page 8, lines 5-10. As shown in FIG. 14 (reproduced below for convenience), the electropolished lower electrode 70 is formed such that it is fully within a contact opening (41, FIG. 7) within insulating layer 25. The capacitor 100 may also include a barrier conductive layer 60 between the insulating layer 25 and the lower electrode 70. A dielectric layer 72 is formed over the lower electrode 70. Upper electrode 74 is formed over dielectric layer 72.

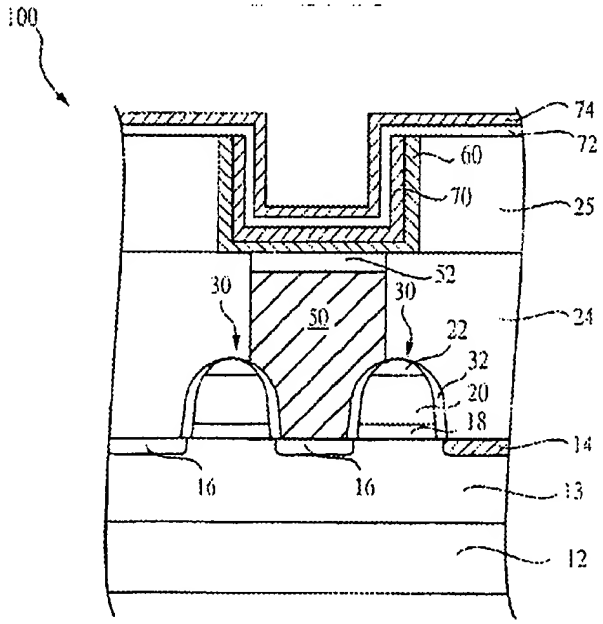

FIG. 14

Claims 55, 56 and 65 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Kirlin et al. (U.S. Patent No. 5,976,928) ("Kirlin"). This rejection is respectfully traversed and reconsideration is respectfully requested.

Claim 55 recites a container capacitor including a "lower electrode provided fully within a first insulating layer, said lower electrode comprising an electropolished patterned metal layer having a bottom wall and vertical sidewalls extending rectangularly upwardly therefrom," a "second insulating layer provided over said electropolished patterned metal layer and in contact with said first insulating layer" and an "upper electrode provided over said second insulating layer."

Applicant respectfully submits that Kirlin does not disclose the "lower electrode comprising an electropolished patterned metal layer having a bottom wall and vertical sidewalls extending *rectangularly upwardly* therefrom" (emphasis added). The capacitor of Kirlin includes bottom electrode 30 having rounded edges. Therefore, it cannot disclose the sidewalls "extending rectangularly upwardly" from the bottom of the electrode. In fact, Kirlin specifically states that the "shape of the capacitor recess 24 will generally be engineered to minimize sharp angles at corners of the three dimensional capacitor structure, in order to prevent cracking of the layers ... or irregular microstructure." Kirlin, col. 9, lines 57-61. Thus, one skilled in the art would not be motivated to modify the structure of Kirlin to form the sidewalls "extending rectangularly upwardly" from the bottom of the electrode. Accordingly, claim 55 is allowable over Kirlin. Claim 56 depends from claim 55 and is allowable along with claim 55.

Claim 65 recites a capacitor structure including an "insulating layer provided over a substrate, the insulating layer including a contact opening, the contact opening having a first height," a "barrier conductive layer provided within the contact opening, the barrier conductive layer being disposed along a bottom and sidewalls of the contact opening, wherein the barrier conductive layer has a first thickness and wherein a length of upwardly extending portions of the barrier conductive layer that are disposed along the sidewalls of the contact opening is equal to the first height," a "lower platinum electrode provided over the barrier conductive layer, the lower platinum electrode being disposed along a bottom portion and sidewall portions of the barrier

conductive layer, wherein a length of upwardly extending portions of the lower platinum electrode that are disposed along the sidewall portions of the barrier conductive layer is equal to the first height minus the first thickness," a "dielectric layer provided over the lower platinum electrode, the dielectric layer being disposed along a bottom portion and sidewall portions of the lower platinum electrode and on an upper surface of the barrier conductive layer and an upper surface of the substrate" and a "second platinum electrode provided over the dielectric layer, the second platinum electrode being disposed along a bottom portion, sidewall portions and an upper surface of the dielectric layer."

Kirlin does not disclose, teach or suggest either that "the dielectric layer [is] disposed along a bottom portion and sidewall portions of the lower platinum electrode and on an upper surface of the barrier conductive layer and an upper surface of the substrate" or that "the second platinum electrode [is] disposed along a bottom portion, sidewall portions and an upper surface of the dielectric layer." As can be seen in FIG. 1H of Kirlin, the top surfaces of each of the bottom electrode 30, the ferroelectric layer 32 and top electrode 34 are even with each other, e.g., at the same height. Ferroelectric layer 32 and top electrode 34 do not extend across the upper surface of the lower electrode. Accordingly, claim 65 is allowable over Kirlin.

Applicant respectfully requests that the rejection of claims 55, 56 and 65 be withdrawn and the claims allowed.

Claims 29-32, 34-39, 41, 44-47, 49, 51-54 and 57-64[1] stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kirlin. This rejection is respectfully traversed and reconsideration is respectfully requested.

Claim 29 recites an intermediate semiconductor device structure[2] comprising a "substrate," an "insulating layer provided over said substrate," an "electropolished patterned metal layer provided within an opening of said insulating layer," and a "photoresist plug provided within

[1] Applicant assumes that, although the rejection is to claims 29-32, 34-39, 41, 44-47, 49, 51-64, claims 55 and 56 are not included in this rejection since these claims are discussed in the 102(e) rejection.
[2] The intermediate structure of claim 29 can be seen, for example, in FIG. 12.

said opening and over and in contact with said electropolished patterned metal layer." The "electropolished metal layer has a thickness of approximately 50 to 300 Angstroms." Also, a "top surface of said electropolished metal layer is electropolished down to said insulating layer so that said top surface of said electropolished metal layer is at the same level with a top surface of said insulating layer."

Claim 36 recites a memory cell comprising a "transistor including a gate fabricated on a semiconductor substrate and including a source/drain region in said semiconductor substrate disposed adjacent to said gate," an "insulating layer provided over said substrate" and a "container capacitor." The capacitor includes a "lower electrode, a dielectric layer over said lower electrode, and an upper electrode over said dielectric layer, said upper electrode comprising doped polysilicon, and said lower electrode having a surface aligned over said source/drain region." The "lower electrode comprises an electropolished patterned metal layer which is situated fully within said insulating layer [and] ... has a thickness of about 50 to about 300 Angstroms." Further, the "dielectric layer is in contact with said insulating layer."

Claim 44 recites a processor-based system including a "processor" and an "integrated circuit coupled to said processor." Further, "at least one of said integrated circuit and said processor compris[e] a container capacitor provided within an insulating layer, said container capacitor including a lower electrode and an upper electrode, said lower electrode comprising an electropolished patterned metal layer having a thickness of approximately 50 to 300 Angstroms, wherein a top surface of said electropolished patterned metal layer is at the same level with a top surface of said insulating layer such that said lower electrode does not extend above the top surface of said insulating layer."

Claim 59 recites a container capacitor including an "insulating layer provided over a substrate, said insulating layer containing an opening," a "tantalum nitride barrier conductive layer provided at a bottom of said opening," a "lower electrode provided over said tantalum nitride barrier conductive layer, said lower electrode comprising an electropolished patterned metal layer having a bottom and vertical sidewalls extending upwardly from said bottom such that said lower electrode is

situated fully within said insulating layer, said lower electrode having a thickness of approximately 100 Angstroms," a "dielectric material provided over said electropolished patterned metal layer and in contact with said insulating layer" and an "upper electrode comprising doped polysilicon provided over said dielectric material." The "lower electrode, said dielectric material and said upper electrode form said container capacitor."

With respect to each of the above claims, the Office Action states that Kirlin teaches all "features except for describing the thicknesses of the metal layer approximately 50-300 Å and a plurality of openings." Office Action, pg. 7. The Office Action further states that the claimed thickness would have been obvious because "where general conditions of a claim are disclosed in the prior [art], discovering the optimum or workable ranges involves only routine skill in the art." Office Action, pg. 5. Applicant respectfully disagrees and submits that the claimed thickness would not have been obvious in view of Kirlin. Kirlin discloses a bottom electrode having a thickness of 0.1 μm (1000 Å), which is one to two times the claimed thickness of the electropolished patterned metal layer.

Additionally, with respect to claim 29, Kirlin does not disclose a "photoresist plug provided within said opening and over and *in contact with* said electropolished patterned metal layer." The buffer layer 35, upon which the Office Action relies as disclosing the photoresist plug, is not in contact with the lower electrode 30.

With respect to claim 36, Kirlin also does not disclose the "lower electrode having a surface aligned over said source/drain region." While Kirlin discusses that conventional circuitry is formed in the substrate (col. 9, lines28-34), Kirlin does not disclose the relative relationship of any possible source/drain region and the lower electrode.

Accordingly, claims 29, 36, 44 and 59 are allowable over the cited combination. Claims 30-32, 34 and 35 depend from claim 29 and are allowable along with claim 29. Claims 37-39 and 41 depend from claim 36 and are allowable along with claim 36. Claims 45-47, 49 and 51-54 depend from claim 44 and are allowable along with claim 44. Claims 57 and 58 depend from claim

55 and are allowable along with claim 55 in addition to the reasons discussed herein. Applicant respectfully requests that the rejection of claims 29-32, 34-39, 41, 44-47, 49, 51-54 and 57-59 be withdrawn and the claims allowed.

In view of the above, Applicant believes the pending application is in condition for allowance.

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Respectfully submitted,

By _____

Gianni Minutoli
Registration No.: 41,198
Jennifer M. McCue
Registration No.: 55,440
DICKSTEIN SHAPIRO LLP
1825 Eye Street, NW
Washington, DC 20006-5403
(202) 420-2200
Attorneys for Applicant